AMENDMENTS TO THE CLAIMS

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. (Currently Amended) A method of Edge-Node Interleave Sort for Leaching and Envelop (ENISLE), comprising:

mapping a circuit into a V-E ~~plain~~ plane, comprised of sides, to transform a circuit information into said V-E ~~plain~~plane which contains the information of node and edge information, ~~Wherein~~ wherein said V indicates nodes that represent components of said circuit and wherein said E indicates edges that represents ~~the~~ nets of said circuits;

determining whether V-E pairs distribution on said V-E ~~plain~~plane is uniform~~ly~~ or not, if said V-E pairs distribution ~~approaching to non-uniformly distribution~~is not uniformly distributed, then randomizing said V-E pairs on said V-E ~~plain~~plane, otherwise performing the following steps for sequentially arranging ~~allocations of~~ the V-E pairs according to the magnitude of each said node or said edge, thereby obtaining min-cut or/and ratio min-cut partitioning;

performing a first sorting step from an edge view based on a first side of said V-E ~~plain~~plane;

performing a second sorting step from ~~an~~ a node view based on a second side of said V-E ~~plain~~plane;

performing a third sorting from said edge view based on a third side of said V-E ~~plain~~plane; and

performing a fourth sorting step from said node view based on a fourth side of said V-E ~~plain~~plane.

2. (Currently Amended) The method of claim 1, wherein said first side refers to a bottom side of said V-E ~~plain~~plane.

3. (Currently Amended) The method of claim 1, wherein said second side refers to a right side of said V-E ~~plain~~plane.

4. (Currently Amended) The method of claim 1, wherein said first side refers to a top side of said V-E ~~plain~~plane.

5. (Currently Amended) The method of claim 1, wherein said first side refers to a left side of said V-E ~~plain~~plane.

6. (Currently Amended) The method of claim 1, further comprising following steps after performing said fourth sorting:

initializing node set record;

performing a fifth sorting step from said node view based on the second side;

performing a sixth sorting step from said edge view based on said first side/third side;

determining whether said node set is still interchanged or not~~? I,~~ if said node set is no longer interchanged, ~~then~~ go back ~~to~~ and perform said fifth sorting step, otherwise, perform~~ing~~ a seventh sorting step from said node view based on said fourth side;

determining whether said node set still interchange or not~~? I,~~ if said node set is still interchanged, then perform~~ing~~ said fifth sorting step for achieving an optimal min-cut or ratio min-cut partitioning.

7. (Currently Amended) The method of claim 6, wherein said first side refers to a bottom side of said V-E ~~plain~~plane.

8. (Currently Amended) The method of claim 6, wherein said second side refers to a right side of said V-E ~~plain~~plane.

9. (Currently Amended) The method of claim 6, wherein said first side refers to a top side of said V-E ~~plain~~plane.

10. (Currently Amended) The method of claim 6, wherein said first side refers to a left side of said V-E ~~plain~~plane.

11. (Currently Amended) A method for min-cut and~~/or~~ ratio min-cut partitioning, comprising:

mapping a circuit into a V-E ~~plain~~plane, comprised of sides, to transform a circuit information into said V-E ~~plain~~plane which contains the information of node and edge information, ~~Wherein~~ wherein said V indicates nodes that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuits;

performing following steps for sequentially arranging ~~allocations of~~ the V-E pairs according to the magnitude of each said node or said edge, thereby obtaining min-cut or/and ratio min-cut partitioning;

performing a first sorting step from an edge view based on a first side of said V-E ~~plain~~plane; performing a second sorting step from an node view based on a second side of said V-E ~~plain~~plane;

performing a third sorting from said edge view based on a third side of said V-E ~~plain~~plane; and

performing a fourth sorting step from said node view based on a fourth side of said V-E ~~plain~~plane.

12. (Currently Amended) The method of claim 11, further comprising determining whether said V-E pairs distribution on said V-E ~~plain~~plane is uniform~~ly~~ or not, if said V-E pairs distribution ~~approaching to non-uniformly distribution~~is not uniformly distributed, then randomizing said V-E pairs on said V-E ~~plain~~plane.

13. (Currently Amended) The method of claim 11, wherein said first side refers to a bottom side of said V-E ~~plain~~plane.

14. (Currently Amended) The method of claim 11, wherein said second side refers to a right side of said V-E ~~plain~~plane.

15. (Currently Amended) The method of claim 11, wherein said first side refers to a top side of said V-E ~~plain~~plane.

16. (Currently Amended) The method of claim 11, wherein said first side refers to a left side of said V-E ~~plain~~plane.

17. (Currently Amended) A method for min-cut and~~/or~~ ratio min-cut partitioning, comprising: mapping a circuit into a V-E ~~plain~~plane, comprised of sides, to transform a circuit information into said V-E ~~plain~~plane which contains the information of node and edge information, ~~Wherein~~ wherein said V indicates nodes that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuits;

determining whether V-E pairs distribution on said V-E ~~plain~~plane is uniform~~ly~~ or not~~,~~; if said V-E pairs distribution ~~approaching to non-uniformly distribution~~is not uniformly distributed, then randomizing said V-E pairs on said V-E ~~plain~~plane, otherwise performing the following steps for sequentially arranging ~~allocations of~~ the V-E pairs according to the magnitude of each said node or said edge, thereby obtaining min-cut or/and ratio min-cut partitioning;

performing a first sorting step from an edge view based on a first side of said V-E ~~plain~~plane;

performing a second sorting step from an node view based on a second side of said V-E ~~plain~~plane;

performing a third sorting from said edge view based on a third side of said V-E ~~plain~~plane;

performing a fourth sorting step from said node view based on a fourth side of said V-E ~~plain~~plane;

initializing node set record;

performing a fifth sorting step from said node view based on the second side;

performing a sixth sorting step from said edge view based on said first side/third side;

determining whether said node set is still interchanged or not~~? If~~, if said node set is no longer interchanged then go back to perform said fifth sorting step, otherwise, perform~~ing~~ a seventh sorting step from said node view based on said fourth side;

determining whether said node set is still interchange or not~~? I~~, if said node set is still interchanged, then performing said fifth sorting step for achieving an optimal min-cut or ratio min-cut partitioning.

18. (Currently Amended) A method for display data compression techniques by different light intensity and/or different patterns on a monochrome viewpoint, comprising:

displaying (V, E) pairs on an initial V-E ~~plain~~plane shown on a monitor screen to observe the said initial (V, E) pairs distributed condition, wherein said V indicates nodes that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuits;

setting L nodes x W edges (V, E) pairs rectangle region to compose a block, wherein said L and W are integers;

defining the more (V, E) pairs in said block to be displayed by the relatively high light intensity to the less (V, E) pairs in said block; and

watching relatively large size of V-E ~~plain~~plane or a whole V-E ~~plain~~plane to said initial (V, E) ~~plain~~plane on said monitor screen, wherein said exact (V, E) pairs positions still be held, thereby zooming in said V-E ~~plain~~plane to watch detail local (V, E) pairs distributed condition, or zooming out to watch global (V, E) pairs distributed condition on said monitor screen.

19. (Currently Amended) A method for display data compression techniques by different light intensity and/or different patterns on a monochrome viewpoint, comprising:

displaying (V, E) pairs on an initial V-E ~~plain~~plane shown on a monitor screen to observe the said initial (V, E) pairs distributed condition, wherein said V indicates nodes that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuits;

setting L nodes x W edges (V, E) pairs rectangle region to compose a block, wherein said L and W are integers;

defining the less (V, E) pairs in said block to be displayed by the relatively high light intensity to the more (V E) pairs in said block; and

watching relatively large size of V-E ~~plain~~plane or a whole V-E ~~plain~~plane to said initial (V, E) ~~plain~~plane on said monitor screen, wherein said exact (V, E) pairs positions still be held, thereby zooming in said V-E ~~plain~~plane to watch detail local (V, E) pairs distributed condition, or zooming out to watch global (V, E) pairs distributed condition on said monitor screen.

20. (Currently Amended) A method for display data compression techniques by different color and/or different patterns on a monochrome viewpoint, comprising:

displaying (V, E) pairs on an initial V-E ~~plain~~plane shown on a monitor screen to observe the said initial (V, E) pairs distributed condition, wherein said V indicates nodes that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuits;

setting L nodes x W edges (V, E) pairs rectangle region to compose a block, wherein said L and W are integers;

defining the more (V, E) pairs in said block to be displayed by the relatively bright color to the less (V, E) pairs in said block; and

watching relatively large size of V-E ~~plain~~plane or a whole V-E ~~plain~~plane to said initial (V, E) ~~plain~~plane on said monitor screen., wherein said exact (V, E) pairs positions still be held, thereby zooming in said V-E ~~plain~~plane to watch detail local (V, E) pairs distributed condition, or zooming out to watch global (V, E) pairs distributed condition on said monitor screen.

21. (Currently Amended) A method for display data compression techniques by different color and/or different patterns on a monochrome viewpoint, comprising:

displaying (V E) pairs on an initial V-E ~~plain~~plane shown on a monitor screen to observe the said initial (V, E) pairs distributed condition, wherein said V indicates nodes

that represent components of said circuit and wherein said E indicates edges that represents the nets of said circuits;

setting L nodes x W edges (V, E) pairs rectangle region to compose a block, wherein said L and W are integers;

defining the more (V, E) pairs in said block to be displayed by the relatively bright color to the less (V, E) pairs in said block; and

watching relatively large size of V-E ~~plain~~plane or a whole V-E ~~plain~~plane to said initial (V, E) ~~plain~~plane on said monitor screen, wherein said exact (V, E) pairs positions still be held, thereby zooming in said V-E ~~plain~~plane to watch detail local (V, E) pairs distributed condition, or zooming out to watch global (V, E) pairs distributed condition on said monitor screen.